

DESIGN OF LITHOGRAPHY ALIGNMENT AND OVERLAY MEASUREMENT  
MARKS ON CMP FINISHED DAMASCENE SURFACE

5    ABSTRACT

          A method for producing a semiconductor device having  
an alignment mark, the method comprising forming a first  
dielectric layer within which a trench having  
predetermined dimensions is etched and depositing a first  
10    layer of metal into the trench; forming a second  
dielectric layer over the first dielectric layer and over  
the first layer of metal; simultaneously etching lines  
and an opening into the second dielectric layer, at least  
one line used as a via extending to the first layer of  
15    metal; filling the lines and the opening, the filling  
controlled to fill the lines and to under fill the  
opening; performing chemical mechanical polishing of the  
plate; and depositing a non-transparent stack of layers  
onto the metal, whereby the non-transparent stack of  
20    layers conforms to the surface of the under filled  
opening resulting in an alignment mark on the non-  
transparent stack of layers in order to align successive  
layers.